Quad Channel IF Receiver Module for Radar Application

Rohit Lahiri[1], Mahadev Sarkar[2] & Gaurav Anand[1]
[1]Microwave Components, Central- D&E,
[2]Control Electronics, Central- D&E,
Bharat Electronics
rohitlahiri@bel.co.in

***Abstract**: This paper describes about design & development of a Quad channel single stage down converter receiver architecture. This receiver module is a part of ERP unit that forms a major entity for Tracking Radar operating at Ka band frequency. The tracking radar front end receiver receives target echo from antenna, amplifies it, and down converts it to IF1 frequency in S band. This forms input to each channel of Quad IF receiver that down converts it to lower IF2 frequency of 120MHz for further processing after amplification & filtering. The major challenge for designing this receiver was to meet key specifications which are Image rejection, Isolation between channels, Gain & phase tracking between channels and Noise figure that were to be met over temperature (-20ºC to +55ºC). This paper gives insight about design considerations to meet some of these key receiver specifications.*

***Keywords:** Exciter-Receiver-Processor(ERP), Super heterodyne Receiver, Spurious, Image frequency, Intermediate Frequency (IF), Local Oscillator (LO), Channel to channel Isolation, GC –Gain Control (i.e. attenuator set to mentioned attenuation value), Vertical Transition.*

I. INTRODUCTION

Radars are used extensively for detection and tracking of targets. Operating frequency of a Radar is selected based on the detection accuracy and applications such as surveillance, tracking, imaging, fire control etc. Therefore, Radars are present across all frequency bands e.g. L, S, C, X etc. Main function of the Radar receiver [1] is to receive weak echo from targets through antenna, amplify the weak echo, filter the unwanted frequencies and down convert the RF Signal to require IF frequency for further processing. In a super heterodyne receiver architecture [2], a Local Oscillator (LO) provides desired frequency band by down-converting the input RF to a fixed IF. This IF is input to digital receiver consisting for further processing. Thus a clean IF signal free from spurious and harmonics is desired for digital processing. Image rejection & out of band filtering are a key feature of a heterodyne receiver to prevent any false target identification. This paper brings out the key design & development features of a Quad IF receiver which down converts from IF1(S band) to IF2 (120MHz), which is input for digital receiver. The realization of receiver is novel & was designed as per governing specifications & system requirements stated by customer.

II. SPECIFICATIONS & DESIGN

The key aspects to be noted while designing a receiver module are its gain, noise figure, image rejection, isolation between receiver channels, phase and amplitude tracking etc. The engineering of the receiver becomes a critical factor in order to meet all the specifications. The specifications of the quad channel IF receiver is shown in Fig-1. The IF1 & LO frequency that are being fed to the receiver are in S band. Output intermediate frequency (IF) from Ka band front end receiver is IF1 frequency fed to Quad channel IF receiver. LO frequency is fed from IF Synthesizer module which is part of ERP unit.

S.N.	Parameter	Specifications
1	Receiver Input Frequency [GHz]	IF1
2	LO Freq [GHz]	LO
3	IF2 Freq	120MHz
4	Number Of Receive Channels	4
5	Noise Figure [GC=10dB]	10dB (max)
6	Nominal Conversion Gain [GC=10dB]	30±1.0dB
7	Isolation B/W Receive Channel	50dB(min)
8	Image Rejection	60 dB (min)
9	Gain Matching B/W Receive Channels	±1.0dB max
10	Phase Matching B/W Rx Channels	±10ºmax
11	Max. Rx I/p Power without damage	+5dBm
12	Max Rx I/p without saturation [GC=10dB]	-20dBm,
13	LO I/P Power Level (LO2_IFRX)	0dBm ± 1dB
14	LO Monitoring Power Level	-10dBm ± 1dB

Fig-1. Critical Specifications for Quad Channel IF Receiver

Based on specifications, block diagram is prepared & cascaded analysis is done to arrive at critical components. The block diagram of receiver is shown in Fig-2

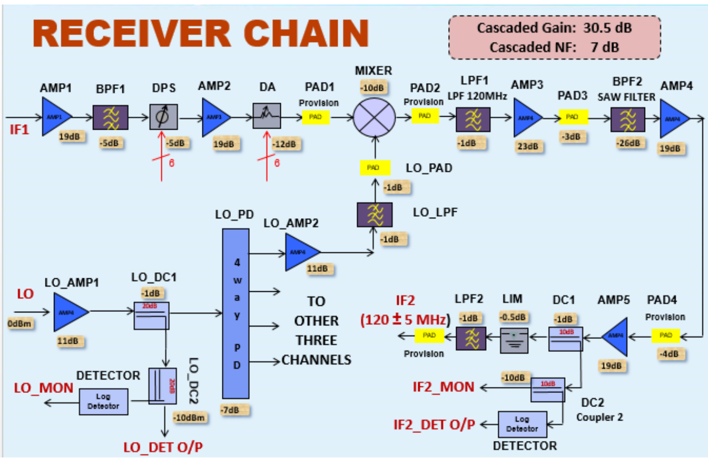

Fig-2. Block diagram of single channel of IF Receiver

It can be noted, that the chain begins with an amplifier. Targeting Noise figure specification, amplifier is chosen in such a way that it can handle more than +5dBm RF I/P which is the damage level for the receiver. Soon after amplifier, an image reject filter is used which aids to achieve minimum of 60dB image rejection spec. To achieve better gain & phase control each receiver channel has a 6 bit digital phase shifter and 6 bit digital attenuator, to meet gain and phase matching specifications. Amplifiers are used in individual LO channels to achieve high isolation of >50 dB in addition to boost LO power level enough to drive mixers. An RF saw filter is used to filter out IF2 frequency after down conversion, and reject any harmonics or spurious generated besides having better group delay in pass band. Detectors are used in both RF & LO path to monitor health status. The cascade analysis of the receiver is carried out with the aid of Cascade Design Suite from Spectrum Microwave and is shown in Fig-3.

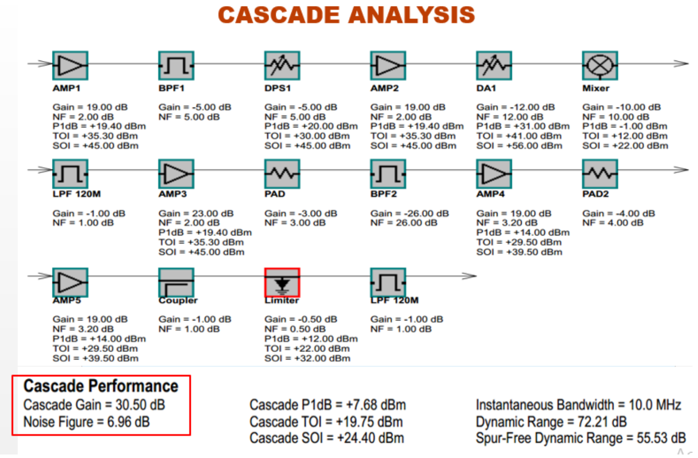

Fig-3. Cascade analysis of receiver chain

As per analysis, RF cascade gain is 30.5dB and noise figure is 7dB with GC=10dB.

III. RECEIVER DESIGN

The quad channel IF receiver consists of three sections: A) Down converter section, B) LO distribution & monitoring section and C) Control & Distribution section. Few passive components like filter, coupler & power divider used in section A & B are simulated using Advanced Design System (ADS) circuit simulator. Sections A, B & C are described below in details:-

A) DOWN CONVERTER SECTION

It is a key section which performs amplification, filtering and down conversion. Single channel RF layout is shown in Fig-4. A modular approach has been implemented where the whole down conversion section is broken into 9 sub-assemblies. Each assembly has carrier plate to support 10mil RF PCB. These are then bridged together using copper stubs. This approach gives advantage that each sub assembly can be tested & replaced separately, without disturbing rest section besides providing flexibility to modify sub-assemblies. This approach also providing additional isolation due to discontinuity is substrate.

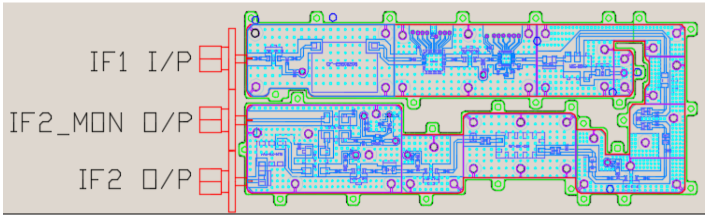

Fig-4. RF layout of Single down converter section

Cavity modelling & resonance analysis of this section is done in 3D EM software (CST Microwave Studio) & is shown in Fig-5. The channelling of this cavity is planned in such a way that the cavity resonates at frequencies that are outside the band of interest. Analysis shows that this cavity resonates at frequency greater than twice IF1 GHz.

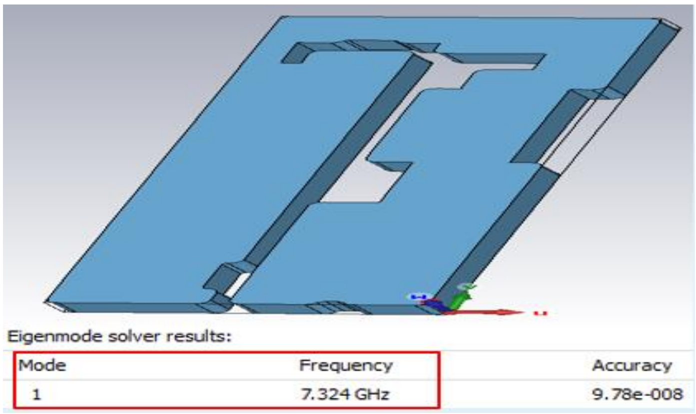

Fig-5. Cavity resonance of single down converter section

B) LO DISTRIBUTION & MONITORING SECTION

The LO input from the IF Synthesizer module (part of ERP unit) is first amplified & then split into four paths using 4 way equal power divider. Amplifiers have also been used in each path of power divider to achieve high channel isolation of >50 dB in addition to boost LO power level enough to drive mixers. LO is fed to down converter section using vertical transitions as shown in Fig-7. LO power monitoring & LO status are also incorporated in this section. LO power is tapped out using coupler and sent to detector (Sub-assembly A) for LO status O/P as seen in Fig-6.

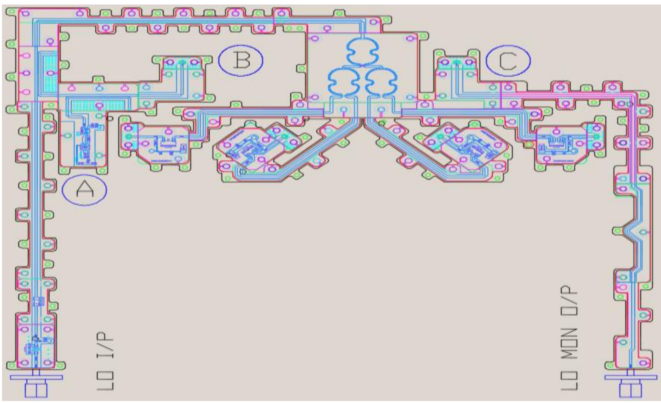

Fig-6. RF layout of LO distribution and monitoring Section

For LO power monitoring, an RF cross-over is bridged using vertical transition [3] simulated in 3D EM software (CST Microwave Studio) as shown in Fig-7. With the aid of transition (sub-assembly B and C) are connected as seen in Fig-6 after crossing to RF side as shown in Fig- 10.

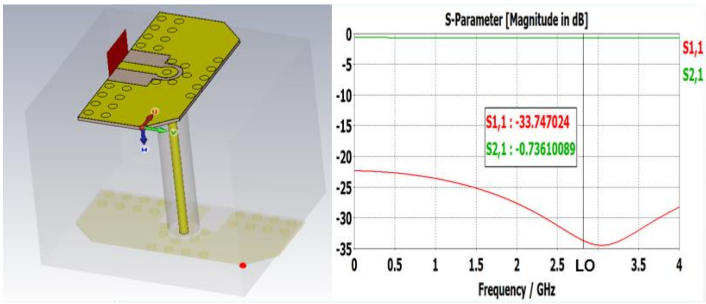

Fig-7. RF vertical transition

The LO distribution & monitoring section has lowest resonant frequency in C band & is almost twice the LO frequency as seen in Fig-8, modelling & simulation done in CST Microwave Studio.

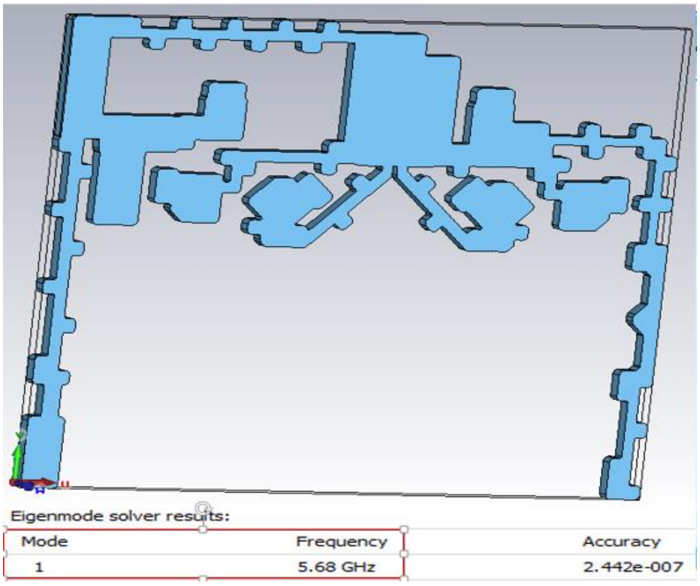

Fig-8. Caity analyis: LO distribution and monitoring Section

C) Power Supply & Control Distribution Section

This is realised on a multilayer FR4 PCB which takes DC input of +5V and -5V from the DC Power Supply Unit & the various LVTTL controls from the TCU unit. These voltages are then distributed to all active devices in the module. It also converts the LVTTL controls to TTL levels & feed to receive channels using buffer amplifiers. The LO and IF status output which are of TTL level is converted back to LVTTL and is sent back. This section is shown in Fig-9. A board mount 62 pin D Sub connector is used as an interface for supply and control signal from mother board of ERP unit.

Fig-9. Power Supply & Control Distribution section

All the three section are combined and integrated together to form working 4 channel IF receiver module and this integration is discussed in next section.

IV. Module Development

Four identical down converter channels can be seen in Fig-10 as RF side (top side of module). Each channel has three BMA connector for blind mating. As shown earlier in Fig-4, these connectors are namely IF1 I/P, IF2 O/P and IF2 MON O/P. After the sub-assemblies are dropped and assembled in overall housing, inner top cover are used in each channel to seal the cavity as shown in Fig-10, thus preventing any RF leakage & providing better isolation.

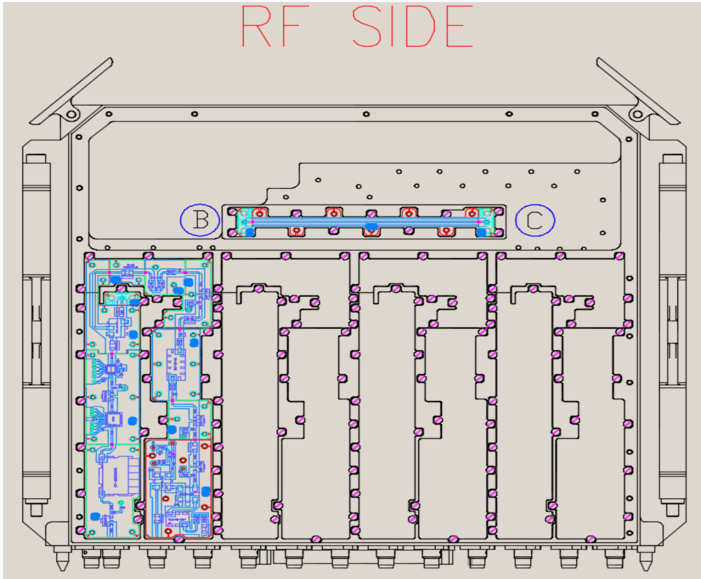

Fig-10. RF Side (Top Side of the module)

The LO and Power Supply side is shown in Fig- 11.Here enamel wires are used to distribute supply & control voltages from power supply & controller board to amplifiers, phase shifters, attenuators & detectors present in each receive channel. Enamel wires are also used to connect Power supply board to LO section to power up all the active devices in LO section. The LO section is also sealed using inner top cover to prevent any leakage.

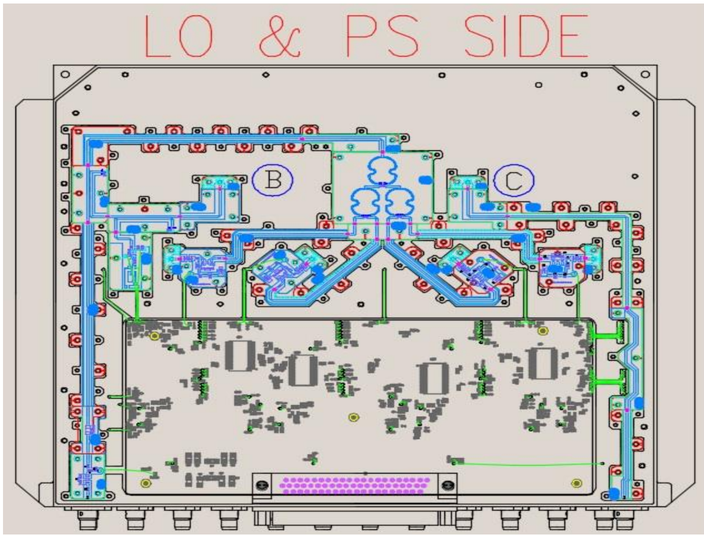

Fig-11. LO & PS Side (Bottom Side of the module)

The developed receiver module is shown in Fig-12. The receiver has been engineered into a mechanical housing of size 190×232×35 mm3. All the input & output connectors have been brought out on same side for blind mating with the mother board of ERP module of Track Radar. Alignment and positioning of connectors has been strategically made for the receiver keeping in mind the width & height of the module and to accommodate 14 BMA connector with a 62 pin D-Sub connector.

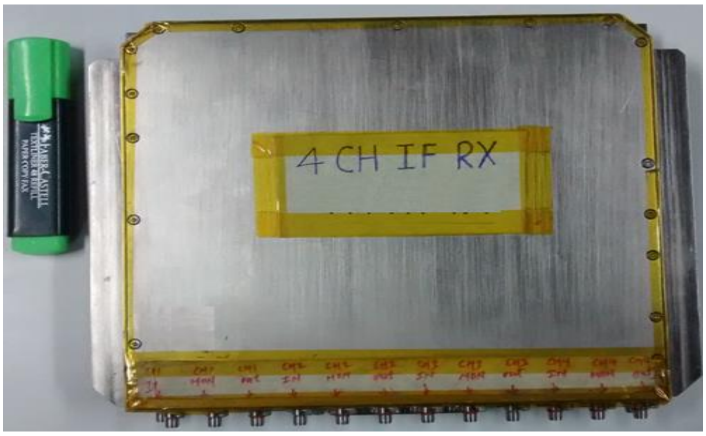

Fig-12. The developed Quad CH IF RX

Evaluation of this module is shown in Fig-13. BMA to SMA adapter cables have been used for mating and testing and 62 pin D sub female connector had been used to feed in supply and control signals to power supply & controller board of Quad receiver during evaluation.

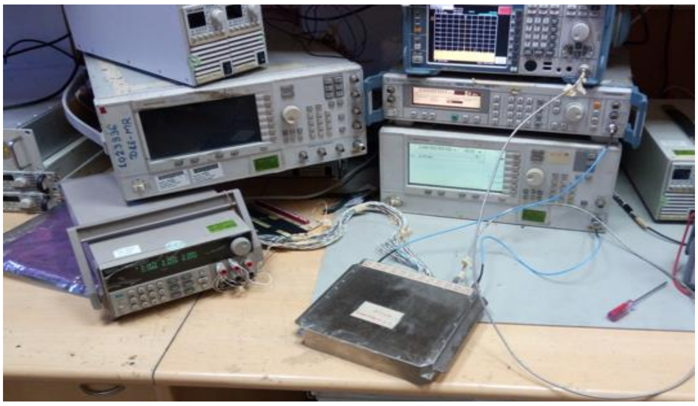

Fig-13. Evaluation of Quad CH IF RX

Gain of each channel, isolation between channels, image rejection, gain & phase tracking, damage level, NF are some of the critical tests performed on this receiver over temperature (-20ºC to +55ºC) and the unit meets the following specifications over this temperature range. Gain of 30±0.8dB with gain control of 10dB, > 57dB isolation, > 62dB image rejection, gain tracking of ±0.8dB max, phase tracking of ±8ºmax, Power level of up to 5dBm RF I/P tested without damaging receiver, and NF of 9.5dB max achieved over temperature.

V. Conclusion

The quad channel IF receiver has been designed and realized with all the three sections (Down converter, LO distribution & monitoring and PS & control distribution section) that are engineered into a mechanical housing of size 190×232×35 mm3 in such a manner that all RF connectors and PS & Control connector are on same side so that it can be plugged into the Exciter-Receiver-Processor (ERP) unit through blind-mating. Gain of each channel in IF receiver module is 30±1dB over temperature (-20ºC to +55ºC) with gain control of 10dB. Image rejection is > 60dB and isolation between channels is > 50dB. Gain matching and Phase matching among channels are ±1dB max and ± 10° max respectively have been achieved. Another key feature of receiver is that, it is modular in approach i.e. each sub assembly can be tested & replaced separately, without disturbing rest section of the receiver besides providing flexibility to modify sub-assemblies.

Acknowledgement

Authors gratefully thank Product design group, C-D&E and Product design group, Military Radar, BEL for providing support for mechanical design & realization. And Microwave Super Components, BEL for facilitating assemblies of the sub modules & integration of receiver module and also providing support for testing. Authors would thank Mr Naresh Kumar, AGM(C-D&E/MWC-1) for encouraging us to carry out this work. Authors would also like to thank all others who were involved directly or indirectly involved in this work.

References

[1] M.Richards, J. A. Scheer, and W. A. Holm, Principle of Modern Radar: Basic Principle. Raleigh, NC, USA: SciTech, 2010.

[2] M. I. Skolnik, “Introduction to Radar Systems”, 2nd Edition, New York: McGraw-Hill, 1980.

[3] G.Anand, R.Lahiri and R.Sadhu, “Wide band microstrip to microstrip vertical coaxial transition for radar & EW applications”, Microwave Conference (APMC), 2016 Asia-Pacific, DOI : 10.1109/APMC.2016.7931432.

Author’s Bio Data

Rohit Lahiri received his B.E. degree in Telecommunication Engineering from M.S. Ramaiah Institute of Technology in year 2011. He joined Bharat Electronics Ltd in same year. Since then he has been part of Central D&E- Microwave Components Group of Bharat Electronics Ltd., Bangalore and at present he is serving there as Senior Engineer. His main research interest is in high frequency and broad band filters, couplers and other passive component designs, besides T/R module & PLL designs. His work includes design & development of wideband microwave components & receiver subsystems for radar & EW applications. He is the recipient of BEL R&D Award 2013.

Mahadev Sarkar completed his B. Tech degree from Murshidabad Engineering College under University of Kalyani, Kolkata and currently pursuing M. Tech & PhD (currently is in halt) in Birla Institute of Technology and Science (BITS) – Pilani. He joined Bharat Electronics in February 2011, and currently working in Broadband Receiver Design projects in Microwave Components group (Central- D&E). Prior to BEL he worked in Powerwave Technologies Research & Development India Pvt. Ltd., Hyderabad in Filters & TMA Design group as Design Engineer-I from 2008 to 2011, and in Astra Microwave Technologies (Unit-III), Hyderabad in core RF Design Group as RF Design Engineer from 2005 to 2008.

Gaurav Anand received his B.E. in Electronics & Communications Engineering from BIT Sindri, Dhanbad in 2003 and M.Tech from IIT Kharagpur in RF & Microwave Engineering in 2006. He is presently working as Manager in Central D&E- Microwave Components Group of Bharat Electronics Ltd, Bangalore. His main research interest is in high frequency and broad band filters, couplers and antenna design. His work includes design & development of wideband microwave components & super components, receiver subsystems and broadband antennas for Radar & EW applications. He is the recipient of BEL R&D Award 2013.